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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/600,737

06/20/2003

Satoshi Ishikura

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12/28/2005

PEARNE & GORDON LLP

1801 EAST 9TH STREET

SUITE 1200

CLEVELAND, OH 44114-3108

EXAMINER

WHITMORE, STACY

ART UNIT

PAPER NUMBER

2825

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary

Application No.

10/600,737

Applicant(s)

ISHIKURA, SATOSHI

Examiner

Stacy A. Whitmore

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 November 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 5-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 5-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 5, 7–9, 15-16, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by lida (US Patent 5,500,542).

2. As for claims 5, 7–9, 15-16 and 18, lida discloses the invention as claimed, including a method or designing, computer readable medium storing a program/ semiconductor device which is formed by (has means or) combining and disposing pre-registered/advance registered functional blocks, and determining a wiring pattern in accordance with a given logic specification, wherein at least one of the functional blocks has a logic circuit and a diode [col. 1, lines 47-57, col. 14, lines 9-14; col. 15, line 45 – col. 16, line 45; figs. 5, 17, 20, 22, 23a – 25b]; and

The diode is composed of a first conduction type diffusion layer and a second conduction type well connected to an input terminal/ power source [col. 1, lines 47-57, col. 14, lines 9-14; col. 15, line 45 – col. 16, line 45; figs. 5, 17, 20, 22, 23a – 25b],
The diode is connected to a potential-clamped input terminal of at least one of the functional blocks [col. 1, lines 47-57, col. 14, lines 9-14; col. 15, line 45 – col. 16, line 45; figs. 5, 17, 20, 22, 23a – 25b; Further see col. 5, line 45 – col. 6, line 22; col. 8, lines 46-50]; and

wherein the diode is connected to a port between an output of the logic circuit and the input terminal of the functional block [col. 1, lines 47-57, col. 14, lines 9-14; col. 15, line 45 – col. 16, line 45; figs. 5, 17, 20, 22, 23a – 25b; Further see col. 5, line 45 – col. 6,

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line 22; col. 8, lines 46-50 – the diode is connected between a plurality of logic circuits and functional blocks and is therefore connected between a port of the output of at least one logic circuit and the input terminal of a functional block].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claim 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over lida (US Patent 5,500,542) in view of Spaanenbergh (US Patent 4,656,592).

4. As for claims 6 and 17, lida discloses the invention substantially as claimed including the semiconductor device as rejected in claim 5 above.

lida does not specifically disclose the logic circuit is a memory.

Spaanenbergh shows a logic circuit being a memory [col. 4].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of lida and Spaanenbergh because utilizing a memory as a logic circuit would provide for storage in a microprocessor system thereby optimizing processing speed of the device [see Spaanenbergh, col. 4, lines 45-55].

5. Claims 10-14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over lida (US Patent 5,500,542) in view of Katsube (US Patent 5,828,119).

6. As for claims 10-14 and 19, lida discloses the invention substantially as claimed, including a method or designing, computer readable medium storing a program/ semiconductor device which is formed by combining and disposing pre-registered/advance registered functional blocks, and determining a wiring pattern in accordance with a given logic specification, wherein at least one of the functional blocks has a logic circuit and a diode [col. 1, lines 47-57, col. 14, lines 9-14; col. 15, line 45 – col. 16, line 45; figs. 5, 17, 20, 22, 23a – 25b]; and

The diode is composed of a first conduction type diffusion layer and a second conduction type well connected to an input terminal/ power source [col. 1, lines 47-57, col. 14, lines 9-14; col. 15, line 45 – col. 16, line 45; figs. 5, 17, 20, 22, 23a – 25b], The diode is connected to a potential-clamped input terminal of at least one of the functional blocks [col. 1, lines 47-57, col. 14, lines 9-14; col. 15, line 45 – col. 16, line 45; figs. 5, 17, 20, 22, 23a – 25b].

lida does not specifically disclose wherein a diode is connected to an input pin where the antenna ratio results exceed an allowed antenna ratio.

Katsube discloses connecting a diode when antenna ratio exceeds an allowed ratio [col. 9, line 49 – col. 10, line 38].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of lida and Katsube because connecting a diode to lida's device when an antenna ratio exceeded an allowed ratio would improve lida's system by preventing a design of a device where the device would be damaged to gate oxide resulting from excess voltage or current or buildup.

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over lida (US Patent 5,500,542) in view of Katsube (US Patent 5,828,119) and further in view of Spaanenberberg (US Patent 4,656,592).

8. As for claim 20, lida in view of Katsube disclose the invention substantially as claimed, including the semiconductor device as rejected above in the rejection of claim 19.

lida in view of Katsube do not specifically disclose that the logic circuit is a memory.

Spaenenberg shows a logic circuit being a memory [col. 4].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of lida in view of Katsube and Spaenenberg because utilizing a memory as a logic circuit would provide for storage in a microprocessor system thereby optimizing processing speed of the device [see Spaenenberg, col. 4, lines 45-55].

9. Applicant's arguments filed November 14, 2005 have been fully considered but they are not persuasive.

In the remarks, applicant argues in substance:

A: lida does not disclose where at least one functional block has logic circuit and a diode.

Examiner respectfully disagrees:

As to A: lida does disclose where at least one functional block has logic circuit and a diode. [see as cited in the rejection of claim 1, and also especially fig. 22 and col. 15, lines 20-35, and therefore reads on the claimed limitations]

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stacy A Whitmore
Primary Examiner
Art Unit 2825



SAW
December 22, 2005